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EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,473	HAN, JONGHEE	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/28/2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10 – 28, 32 – 40 and 42, are rejected under 35 U.S.C. 102(b) as being anticipated by Park.

4. Examiner makes a note in regards to better understanding the rejection of claims 10, 16, 27, 32 and 39. In order to better assist the applicant to understand the Park reference the examiner makes note of the correlation of Park with the related art (figure 1). As described by Park in column 2, lines 36 – 47 Park's invention modifies related art

in order to support a mode that is synchronized to both side edges of the system clock and the corresponding frequency. Therefore Park includes the teachings of the related art, as it is a modification of it. Additionally in Park figure 1, elements 101, 102, 110, 240, 242, map to the applicant's figure 1 elements 101, 104, 110, 108, 107 respectively.

5. As per claim 10 Park teaches a method comprising,

driving a first data on a data bus (FRDB, column 4, lines 40 – 42);

issuing (first Enable, column 7 lines 1 – 16)a strobe signal from a controller (FRDB strobe signal, column 4, lines 40 – 42);

receiving, by a receiving circuit (receiver), the strobe signal a period of time after issuing the strobe signal; in response to receiving the strobe signal by the receiving circuit, latching in the first data from the data bus (FRDB latch, element 41, figure 2, column 4 line 39);

receiving, by the controller, the strobe signal a period of time after issuing the strobe signal (SRDB latch, element 42, figure 2, column 4, line 47); and

in response to receiving the strobe signal by the controller, driving a second data on the data bus (along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1).

6. As per claim 11, Park teaches a method wherein (a)-(f) are performed bidirectionally over the data bus (element 105, figure 1).

7. As per claims 12 and 17 Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line (database controlling unit, element 34, figure 2, column 6, lines 38 – 61).

Database controlling unit taught by Park, tied into the FIFO unit element 35 of figure 2 and the latency pipeline controlling unit element 36 of figure 2 allow for sharing a common line in a portion.

8. As per claim 13, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein lengths of the first and second paths are substantially the same (column 6, lines 50 – 67).

9. As per claim 14, Park teaches a method comprising, latching the second data in from the data bus (SRDB latch, element 42, figure 2, column 4, line 47).

10. As per claim 15 Park teaches a method wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

11. As per claim 16, Park teaches a method comprising:

(1) by a driver controller (element 34, figure 2): driving first data on a data bus (FRDB, column 4, lines 40 – 42); transmitting a data strobe signal to a receiver via a forward signal path (FRDB strobe signal, column 4, lines 40 – 42); receiving the data strobe signal via a return signal path; and in response to receiving the strobe signal, driving second data on the data bus (SRDB, column 4, lines 43 – 44); and (2) by a receiver (data path composition 32, figure 2): receiving the strobe signal via the forward signal path (FRDB strobe signal, column 4, lines 40 – 42); and in response to receiving the strobe signal, latching the first data in from the data bus(FRDB latch, element 41, figure 2, column 4 line 39).

12. As per claim 28, Park teaches a device wherein the round-trip path is partially defined by the strobe clock signal line (column 6, 42 – 60, controller round- trip path).

13. As per claim 32, Park teaches a circuit comprising:

a controller comprising a strobe clock signal output (strobe signal, column 4, lines 40 – 45) and a return clock signal input and configured to issue a first enable signal (first Enable, column 7 lines 1 – 16) and a second enable signal (second Enable, column 7 lines 1 – 16), the first enable signal enabling a plurality of drivers to drive respective first data on respective data lines, and the second enable signal enabling the plurality of drivers to drive respective second data on their respective data lines;

a strobe clock signal line coupled to the strobe clock signal output (SDO, column 4, lines 45 – 50); and

a return clock signal line coupled to the return clock signal input; wherein the strobe clock signal line defines an initial portion of a round-trip path and the return clock signal line defines a terminal portion of the round-trip path; and wherein the controller is configured to (column 5, lines 20 – 26);

respond to an external clock signal by pulling a strobe clock signal to a first state on the strobe clock signal line and pulling the first enable signal to an active state (column 7, lines 1 – 10);

receive a return clock signal on the return clock signal line a period of time after pulling the strobe clock signal to the first state, wherein the return clock signal is timed off of the strobe clock signal and indicates an assumed receipt of the strobe clock signal in the active state by receiving circuitry coupled to the respective data lines and configured to latch in the first (FRDB latch, element 41, figure 2, column 4 line 39) and second (SRDB latch, element 42, figure 2, column 4, line 47) data from the data lines in response to the strobe clock signal; and

respond to the received return clock signal by pulling the second enable signal to an active state (column 7, line 4).

14. As per claim 33, Park teaches a circuit wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM, column 4, lines 14 – 16).

15. As per claim 34, Park teaches a circuit wherein the strobe clock signal is coupled to the return clock signal line and to the receiving circuitry (elements 41 and 42, figure 2, coupled to FSRDB for receiving).

16. As per claim 35, Park teaches a circuit wherein the receiving circuitry is configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) in the first data from the data lines in response to receiving the strobe clock signal in the first state and to latch (SRDB latch, element 42, figure 2, column 4, line 47) in the second data from the data lines in response to receiving a transition of the strobe clock signal from the first state to a second state.

17. As per claim 36, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 60 – 65).

18. As per claim 37, Park teaches a circuit wherein the strobe clock signal and the return clock signal are issued within a single period of an external clock signal (element 33, figure 2, column 5, lines 19 - 29).

19. As per claim 38, Park teaches a circuit wherein the return clock signal is a delayed instance of the strobe clock signal (element 33, figure 2, column 4, lines 55 – 65).

20. As per claim 39 Park teaches a device comprising,

In order to better assist the applicant to understand the Park reference the examiner makes note of the correlation of Park with the related art (figure 1). As described by Park in column 2, lines 36 – 47 Park's invention modifies related art in order to support a mode that is synchronized to both side edges of the system clock and the corresponding frequency. Therefore Park includes the teachings of the related art as it is a modification of it. Additionally in Park figure 1, elements 101, 102, 110, 240, 242, map to the applicant's figure 1 elements 101, 104, 110, 108, 107 respectively.

a bidirectional data bus (element 105, figure 1);

a first driver circuit coupled to the bus (FRDB, column 4, lines 40 – 42) and configured to propagate a first data and a second data in a first direction along the bus;

a first receiver circuit coupled to an end of the bus opposite the first driver circuit and configured to latch (FRDB latch, element 41, figure 2, column 4 line 39) the first and second data in response to a first strobe clock signal (FRDB strobe signal, column 4, lines 40 – 42);

a second driver circuit coupled to the bus (SRDB, column 4, lines 43 – 44) and configured to propagate a third data and a fourth data in a second direction along the bus;

a second receiver circuit coupled to an end of the bus opposite the second driver circuit and configured to latch (SRDB latch, element 42, figure 2, column 4, line 47) the

third and fourth data in response to a second strobe clock signal (along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1);

a first controller configured to enable the first driver circuit and to generate the first strobe clock signal (first Enable, column 7 lines 1 – 16);

a second controller configured to enable the second driver circuit and to generate the second strobe clock signal (second Enable, column 7 lines 1 – 16);

a first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) to propagate the first strobe clock signal from the first controller to the first receiver circuit;

a first round-trip path comprising a first return path for the first strobe clock signal back to the first controller (column 6, 42 – 60, controller round-trip path, along the bidirectional bus between the I/O interface 110 and connecting circuit, figure 1);

a second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45) to propagate the second strobe clock signal from the second controller to the second receiver circuit; and

a second round-trip path comprising a second return path for the second strobe clock signal back to the second controller (column 6, 42 – 60, controller round-trip path).

21. As per claim 40, Park teaches a device wherein the first round-trip path is partially defined by the first strobe clock signal line (FRDB strobe signal, column 4, lines 40 – 42) and the second round-trip path is partially defined by the second strobe clock signal line (SRDB strobe signal, column 4, lines 43 – 45).

22. As per claim 42, Park teaches a device wherein the first strobe clock signal line comprises at least a portion of the second strobe clock signal line (database controlling unit, element 34, figure 2, lines 35 – 50).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 1 – 9 and 29 – 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US Patent Number 6,147,926) in view of Dao et al (US Publication Number 2006/0236018, hereinafter "Dao").

25. As per claim 1, Park teaches a method comprising:

driving first data on a data bus;

transmitting, via a first signal path (FRDB, column 4, lines 40 – 42), a strobe signal to a receiving circuit indicating the validity of the first data on the data bus (database controlling unit transmits SDO valid signal indicating validity of data, column 4, lines 35 – 56); and

in response to receiving the return signal (FRDB latch, element 41, figure 2, column 4 line 39), driving second data on the data bus (SRDB, column 4, lines 43 – 44).

Park teaches validity verification (valid signal, figures 2 and 3), however does not explicitly disclose the newly amended claim limitations of receiving a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit.

Dao teaches in an analogous DDR SDRAM environment (paragraph [0147]), a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit (multiple acknowledgement return strobe signals, paragraphs [0207,0215,0234,0246]).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Park with the above teachings of Dao. One of ordinary skill would be motivated to make such modifications in order to optimize transaction data forwarding (paragraph [0168]).

26. As per claim 2, Park teaches a method wherein driving the first data and the second data on the data bus comprises enabling a driver to drive the data (output driver, element 44, figure 2, column 4, lines 55 – 65).

27. As per claim 3, Park teaches a method wherein the data bus is an internal data bus of the multiple data rate memory device (column 4, lines 1 – 20).

The data bus taught by Park is internal to the DDR SDRAM thus internal to the memory device.

28. As per claims 4 and 31, Park teaches a method wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

29. As per claims 5 and 30, Park teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 4, lines 63 – 65).

30. As per claim 6, Park teaches a method wherein; a duration of time between issuing the strobe signal and receiving the return signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 5, lines 1 – 7).

31. As per claim 7, Park teaches a method wherein the return signal is the strobe signal (column 4, lines 40 – 48, strobe signals).

32. As per claim 8, Park teaches a method further comprising generating the return signal by the receiving circuit (column 6, lines 27- 29 & 45 – 53).

33. As per claim 9, Park teaches a method wherein generating the return signal comprises buffering the strobe signal (output buffer, element 44, figure 2, column 5, lines 12 – 17).

34. As per claim 18, Park teaches a method comprising:

enabling a driver to drive a first data on a data bus (first Enable & second Enable, column 7 lines 1 – 16);

issuing a strobe signal to a receiving circuit via a forward signal path to indicate the presence of the first data on the data bus (FRDB strobe signal, column 4, lines 40 – 42);

in response to receiving the return signal (FRDB latch, element 41, figure 2, column 4 line 39), driving second data on the data bus (SRDB, column 4, lines 43 – 44).

Park teaches validity verification (valid signal, figures 2 and 3), however does not explicitly disclose the newly amended claim limitations of receiving a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit.

Dao teaches in an analogous DDR SDRAM environment (paragraph [0147]), a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit (multiple acknowledgement return strobe signals, paragraphs [0207,0215,0234,0246]).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Park with the above teachings of Dao for the same reasons shown above in claim 1.

35. As per claim 19, Park teaches a method wherein a duration of time between issuing the strobe signal and receiving the return signal is at least as long as a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 4, lines 63 – 65).

36. As per claim 20, Park teaches a method wherein; a duration of time between issuing the strobe signal and receiving the return signal is substantially equal to a duration of time required for the strobe signal to propagate from the control circuit to the receiving circuit (element 33, figure 2, column 5, lines 1 – 7).

37. As per claim 21, Park teaches a method wherein receiving the strobe signal by the control circuit occurs substantially simultaneously with receipt of the strobe signal by the receiving circuit (database controlling unit, element 34, figure 2, column 6, lines 39 – 53).

38. As per claim 22, Park teaches a method wherein the data bus is an internal data bus of the multiple data rate memory device (column 4, lines 1 – 20).

The data bus taught by Park is internal to the DDR SDRAM thus internal to the memory device.

39. As per claim 23, Park teaches a method comprising, within the given clock period, driving the first data on the data bus (FRDB, column 4, lines 40 – 42).

40. As per claim 24 Park teaches a method wherein the multiple data rate memory device is a double data rate synchronous dynamic random access memory (DDR SDRAM) (DDR SDRAM, column 4, lines 14 – 16).

41. As per claim 25, Park teaches a method wherein the strobe signal is propagated to the receiving circuit on a first path and propagated to the controller on a second path, and wherein only a portion of each path shares a common line (database controlling unit, element 34, figure 2, column 6, lines 38 – 61).

Database controlling unit taught by Park, tied into the FIFO unit element 35 of figure 2 and the latency pipeline controlling unit element 36 of figure 2 allow for sharing a common line in a portion.

42. As per claim 26, Park teaches a method, wherein the first line is couple to the receiving circuit (FRDB latch, element 41, figure 2, column 4 line 39).

43. As per claim 29 Park teaches a device comprising:

a driver configured to drive at least a first data and a second data (FRDB, column 4, lines 40 – 42);

a receiver coupled to the driver (FRDB latch, element 41, figure 2, column 4 line 39);

a controller coupled to the driver and configured to enable the driver to drive the first data and the second data (first Enable & second Enable, column 7 lines 1 – 16);

a strobe clock signal line coupled between the receiver and controller and configured to propagate a strobe clock signal (FRDB strobe signal, column 4, lines 40 – 42).

Park teaches validity verification (valid signal, figures 2 and 3), however does not explicitly disclose the newly amended claim limitations of receiving a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit.

Dao teaches in an analogous DDR SDRAM environment (paragraph [0147]), a return signal in the form of the strobe signal transmitted via a second signal path, the arrival of the return signal indicating an (assumed) arrival of the strobe signal at the receiving circuit (multiple acknowledgement return strobe signals, paragraphs [0207,0215,0234,0246]).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings of Park with the above teachings of Dao for the same reasons shown above in claim 1.

In order to better assist the applicant to understand the Park reference the examiner makes note of the correlation of Park with the related art (figure 1). As described by Park in column 2, lines 36 – 47 Park's invention modifies related art in order to support a mode that is synchronized to both side edges of the system clock and the corresponding frequency. Therefore Park includes the teachings of the related art as it is a modification of it. Additionally in Park figure 1 elements 101, 102, 110, 240, 242 map to the applicant's figure 1 elements 101, 104, 110, 108, 107 respectively.

Response to Arguments

44. Applicant's arguments with respect to claims 1, 18 and 29 have been considered but are moot in view of the new ground(s) of rejection.

45. Applicant's arguments filed 10/30/2006 with respect to claims 10, 16, 27, 32 and 39 have been fully considered but they are not persuasive. The Applicant argues for claims 10 and 16: Park does not disclose providing a return/round trip path for a strobe signal and controlling the driving/latching of first and second data in response to receiving the strobe signal via the return path.

46. As per the arguments with respect to claim 10, the Examiner respectfully disagrees. The applicant argues limitations not necessitated by the claims and notes that the features upon which applicant relies (i.e., providing a return path for a strobe

signal and controlling the driving/latching of first and second data in response to receiving the strobe signal via the return path.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

47. As per the argument with respect to claim 16, 27 and 39, the Examiner respectfully disagrees. Park teaches a round trip path in the form of QCLK sync unit 53 in figure 4 that manages a strobing return clock signal back to the controller. The bidirectional bus interface figure 1 from element 102 reinforces the two-direction/return path configuration that Park's modification utilizes in enhancement. The clock sync unit is internal to the latency unit that directly corresponds to the database-controlling unit (column 5, lines 19 – 34). Clearly from this citation, one of ordinary skill in the art would recognize that the controller has a return path on which a return strobe clock signal is present.

48. As per the arguments with respect to claim 32, the Examiner respectfully disagrees. The applicant argues limitations not necessitated by the claims and notes that the features upon which applicant relies (i.e., a round trip path comprising a return path for the strobing clock signal back to the controller) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from

the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER

3/2/07